ABSTRACT OF THE DISCLOSURE

A decoder generally comprising a branch metrics circuit and a state metrics circuit. The branch metrics circuit may be configured to generate a plurality of branch metric signals. The state metrics circuit may be configured to (i) add the branch metric signals to a plurality of state metric signals to generate a plurality of intermediate signals, (ii) determine a next state metric signal to the state metric signals, (iii) determine a normalization signal in response to the intermediate signals, and (iv) normalize the state metric signals in response to the normalization signal.